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Attaining Melt Processing of Complementary Semiconducting Polymer Blends at 130 °C via Side-Chain Engineering

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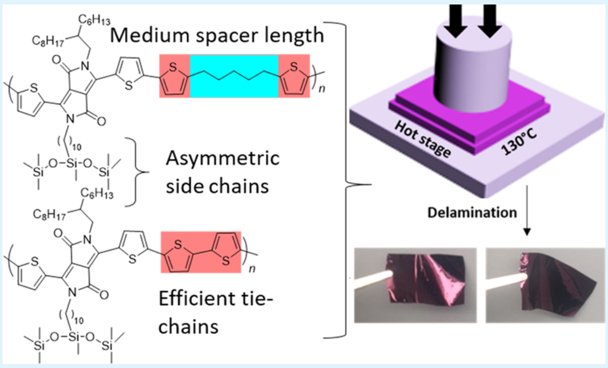
Supporting Information

ABSTRACT: Complementary semiconducting polymer blends (c-SPBs) have been proposed and tested to achieve melt-processed high-performance organic field-effect transistors (OFETs). Prior to this study, melt processing requires temperatures as high as 180 °C. To implement this technique into low-cost and large-area thin-film manufacturing for flexible organic electronics, semiconducting materials meltable at temperatures tolerable by ubiquitous plastic substrates are still needed. We report here the design and melt processing of a c-SPB consisting of a matrix polymer (DPP-C5) and its fully conjugated analogue. By utilizing a siloxane-terminated alkyl chain and a branched alkyl chain as solubilizing groups, the matrix polymer DPP-C5 presents a melting temperature of 115 °C. The resulting c-SPB containing as low as 5% of the fully conjugated polymer could be melt-processed at 130 °C. The obtained OFET devices exhibit hole mobility approaching 1.0 cm^2/(V s), threshold voltages below 5 V, and I_{ON}/I_{OFF} around 10^5. This combination of efficient charge-carrier transport and considerably low processing temperatures bode well for melt processing of semiconducting polymer-based organic electronics.



KEYWORDS: *melt processing, semiconducting polymers, side-chain engineering, organic field-effect transistors, low processing temperature*

INTRODUCTION

Organic field-effect transistors (OFETs) represent a promising alternative in designing integrated circuits for various applications in flexible electronics.[1−5] Solution-processable organic semiconductor materials have been used to achieve high performance required for practical applications.[6,7] OFETs have seen tremendous improvement in the past several years, surpassing the required mobilities for many device applications and even approaching the performance of amorphous silicon-based counterparts.[8,9] Solution processing has thus been an appealing route for thin-film formation in device fabrication as it can be easily achieved with high speed under ambient conditions; it has been envisioned to be a presumptive method for roll-to-roll printing. However, this approach is still plagued with some practical issues, such as the environmental issue, as most high-performing semiconductor polymers are mostly soluble in chlorinated solvents,[10,11] and poor morphology control, as the solvent evaporation rates dominate the film formation.[12,13]

To obviate these complications raised by the use of solvents, one of the proposed fabrication routes is solvent-free processing. For instance, methods such as melt processing, friction-transfer technique, and high-temperature rubbing have been demonstrated to be feasible in thin-film transistor fabrication.[14−16] Melt processing approach remains less appealing because most high-performing materials used in OFETs can only be melted at rather high temperatures.[16,17] In efforts to circumvent high-temperature ramping, polymer systems, such as regioregular polythiophenes, have been demonstrated to be blended with insulating matrices and achieve high-performance devices at considerably low processing temperatures.[18,19] In the first scenario, vertical phase segregation is often observed and utilized as a mean to increase the overall device performance by inducing crystallization of the semiconducting polymer within insulating matrices.[9,20−23] By blending low-performance semiconducting polymers (e.g., P3HT with insulating polymer matrices), in the second scenario, the induced crystallization can allow the formation of highly aligned nanowires, which leads to an increase in charge-carrier transport by several orders of magnitude, thereby achieving lowered processing temperatures.[19,23,24] These blending systems show promising device performances to serve as a material platform for melt processing; however, achieving the morphological stability and high charge-carrier mobility are challenging. For instance, melt crystallization will lead to undesired phase segregation.[16,25−27] There thus seems

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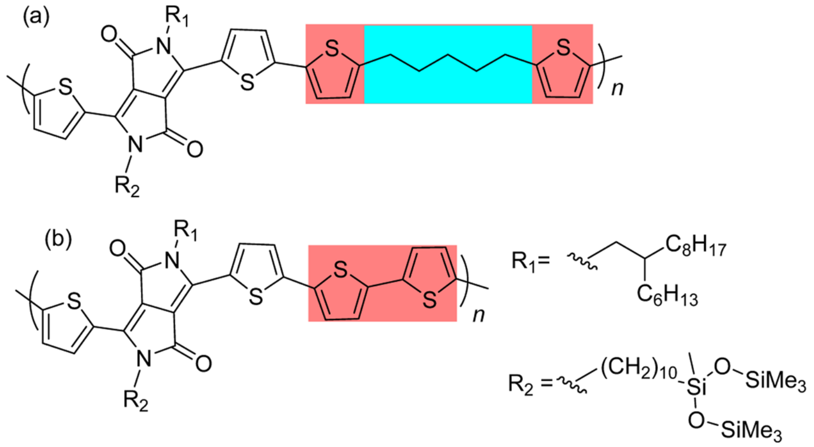

Figure 1. Molecular structures of (a) the matrix polymer: Si-C1C6C8-DPP-C5 and (b) the tie chain polymer: Si-C1C6C8-DPP-C0.

to be a lack of a semiconducting system that is both intrinsically high-performing and readily melt-processable.

Our research group has recently demonstrated a different approach to avoid phase segregation in melt processing by employing complementary semiconducting polymer blends (c-SPBs).[28] Zhao et al. reported a matrix polymer with a pentamethylene (C5) conjugation-break spacer utilized to be blended with a small portion of its fully conjugated analogue. This binary system showed no phase separation and excellent morphology stability due to structural complementarity between the tie polymer and the host matrix. However, the melt processing of this pair could only be realized at elevated temperatures (160 °C and above) as the matrix polymer alone melts around 140 °C. Such a high temperature makes it difficult to integrate these blends to low-cost, large-scale printing techniques, where low processing temperatures[4] (typically lower than 150 °C) are desired. For instance, Zardetto et al. demonstrated that the physical and electrical properties of most commonly used substrates (as well as their indium tin oxide (ITO)-modified analogues) can be greatly impeded at temperatures above 150 °C.[29] Both poly(ethylene terephthalate) and poly(ethylene naphthalate), two of the most commonly used substrates, showed to start bending upon thermal treatment higher than 150 °C. More importantly, the ITO-modified sheets of these polymer substrates showed an exponential increase in electrical resistance concomitant to the bending.[29] To attain this substrate−semiconductor compatibility, lower processing temperatures, lower than 150 °C, would be ideal. Besides, lowering the processing temperatures would translate to reducing the inherent energy consumption associated with the use of high-temperature ramping for large-scale manufacturing. To make melt processing a promising and potential candidate for organic electronics and to fulfill an easier, greener, and low-cost processing, lower-melting-point and high-performance semiconducting polymer systems are still urgently needed. Achieving such a semiconducting system would obviate the need for post-processing treatment steps and allow for the practical use of melting in electronic thin-film manufacturing.

One way to lower the melting temperatures of the matrix polymers would be to increase the spacer length, but semiconducting properties would then be compromised.[30] Alternatively, side-chain engineering has been demonstrated by our group as a tool to tune the melting point of matrix polymers.[31] Notably, the use of asymmetric side chains showed to yield lower melting temperature for a DPP matrix polymer with five methylene units. Here, we report the design and melt processing of c-SPBs consisting of a DPP-C5 matrix bearing asymmetric side chains as solubilizing groups and its fully conjugated analogue. With a siloxane-terminated alkyl chain on one side and a branched alkyl chain on the other side, the matrix polymer showed a melting temperature as low as 115 °C. Melt-processed OFET devices of the resulting c-SPBs with charge-carrier mobilities approaching 1.0 cm^2/(V s), I_{ON}/I_{OFF} greater than 10^5, and threshold voltage below 5 V could be fabricated at 130 °C with no post-treatment steps required. To our knowledge, this is the first intrinsically semiconducting polymer system to be melt-processed at such low temperatures with such electrical and film stability behavior. By combining the ability to be melt-processed at significantly low temperatures and the potential to yield high-performance OFET devices, this system opens the door for robust and sustainable processing routes in organic electronic thin-film manufacturing.

■ RESULTS AND DISCUSSION

Materials Design, Synthesis, and Characterization. As previously demonstrated, conjugation break spacers can be used to tune polymer backbone flexibility as well as their melting temperatures. Zhao et al. demonstrated that π-conjugation in semiconducting polymers can be intentionally interrupted by placing an alkyl chain along the polymer backbone, yielding melt-processable semiconducting polymer thin films and fibers.[30,32] In a subsequent study, we demonstrated that asymmetric side chains could yield lowered melting transitions for the same polymer backbones.[31] In this study, a DPP-based matrix polymer with a five-carbon (five methylene units) flexible spacer affording sufficient backbone flexibility was selected.[30,31,33] A branched alkyl chain placed two carbons away from the backbone (C1C6C8−) and an elongated alkyl chain with a siloxane terminal group (Si−) were then used as the solubilizing chains. This breaking of symmetry in side chains has been also recently found to be beneficial for yielding mixed orientations and improved charge transport in isoindigo-based donor−acceptor systems.[34] The molecular structure of the matrix polymer, Si-C1C6C8-DPP-C5, is shown in Figure 1a. The same solubilizing side chains were then utilized for the fully conjugated (tie-chain) polymer, which was subsequently chosen to make the corresponding melt-processable blends. The complementary tie-chain polymer, Si-C1C6C8-DPP-C0, is shown in Figure 1b. Both polymers were prepared as previously reported[30,35] and were fully characterized using NMR, UV−vis

Table 1. Physical Characterization of Si-C1C6C8-DPP-C5, Si-C1C6C8-DPP-C0, and Their 5% c-SPB

material	M_n (kDa)/$Đ$	T_d (°C)	T_m (°C)	λ_{max} (nm) solution[b]	λ_{max} (nm) film[c]	energy levels (eV) E_{HOMO}[d]	energy levels (eV) E_{LUMO}[e]
Si-C1C6C8-DPP-C5	19.1/1.2[a]	411	125	589, 626	591, 628	−5.19	−3.81
Si-C1C6C8-DPP-C0	5.8/1.2[f]	417		733, 799	749, 822	−4.95	−3.55
5% c-SPB	NA	417	132	618, 671	622, 674		

[a] Tetrahydrofuran is used as the eluent at room temperature. [b] Chloroform used as the solvent. [c] Drop-casted films on glass substrates. [d] Obtained from ultraviolet photoelectron spectroscopy, uncertainty ±0.05 eV. [e] Calculated using the equation $E_{LUMO} = E_{HOMO} + E_g^{opt}$. [f] Trichlorobenzene used as the eluent at 150 °C.

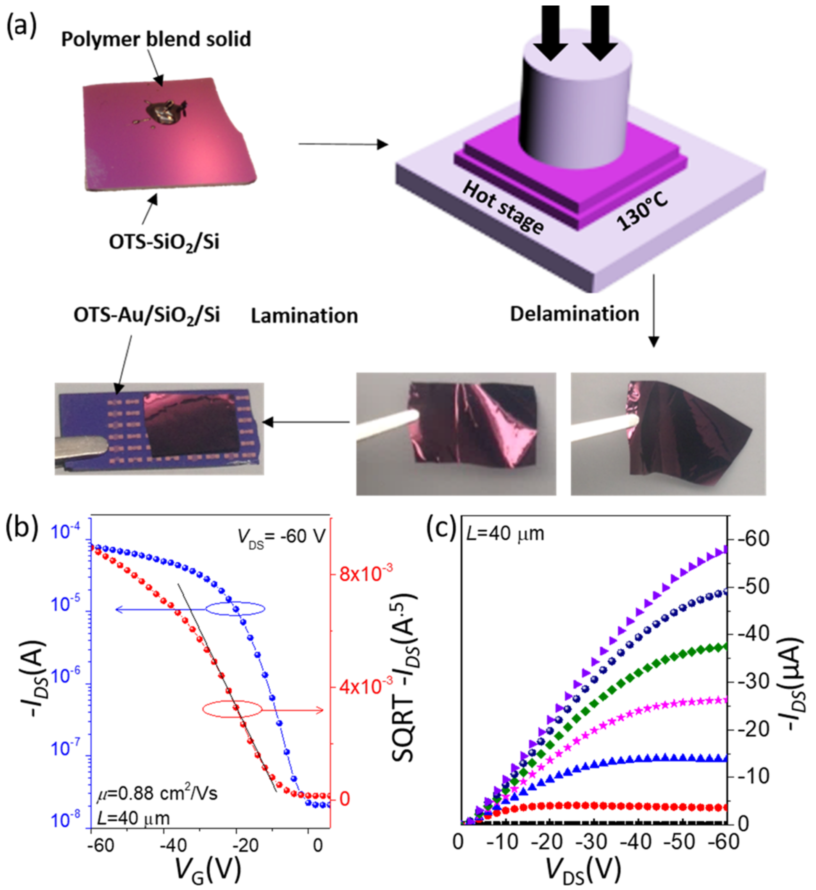

Figure 2. (a) Illustration of the thin film formation by melt pressing and OFET fabrication by delamination−lamination method. Characteristic transfer (b) and output (c) curves of the best-fabricated OFET device based on the polymer c-SPB.

absorption, and gel permeation chromatography. The characterization results can be found in the Supporting Information, and the physical properties are summarized in Table 1.

Physical blends of Si-C1C6C8-DPP-C5 and Si-C1C6C8-DPP-C0 were used to demonstrate the melt processing of OFET devices. From differential scanning calorimetry (DSC) (the second cycle) results (Figure S5), Si-C1C6C8-DPP-C5 showed a melting transition with the peak maximum around 125 °C. By blending 5% of the tie chains into the matrix polymer, the designed blend system showed a melting point slightly higher than that of the pure matrix with a peak maximum shift of ~7 °C. The fully conjugated polymer did not show any notable thermal transitions before 350 °C. Thermogravimetric analysis showed that Si-C1C6C8-DPP-C0 is thermally stable up to 417 °C (Figure S4). This thermal behavior of 5% c-SPB different from that of the pure matrix polymer is an indication of the lack of polymer phase separation, which is in good agreement with previously reported DPP-based blends. The 5% c-SPB was further utilized to investigate the melt processing of OFET devices at temperatures near the melting point of the blend system.

OFET Characterization. Melt-processed devices were fabricated as follows.[28] Briefly, Si/SiO$_2$ substrates with Au electrodes were first cleaned using piranha solution (2 vol 18 M sulfuric acid: 1 vol 30% hydrogen peroxide), followed by copious rinsing with water and then sonicated in isopropanol and acetone each for 5 min. The cleaned and dried substrates were then modified with a self-assembled monolayer of octadodecyltrichlorosilane (OTS). Bottom gate, bottom contact OFET devices were then fabricated by melt processing inside a N$_2$ glovebox, as illustrated in Figure 2a. The polymer blends were first allowed to mix in their solutions. Approximately 5 mg of the dried blended solid was used to form a thin film of a polymer blend by melting at 130 °C inside the N$_2$ glovebox.

Table 2. Representative OFET Parameters for Devices Based on the Pure Matrix Polymer (Si-C1C6C8-DPP-C5), the Tie-Chain Polymer (Si-C1C6C8-DPP-C0), and the Resulting c-SPB when 5, 10, and 50 wt % of Si-C1C6C8-DPP-C0 are Used

material	μ_{max} (cm^2/(V s))	μ_{avg} (cm^2/(V s))	V_{th} (V)	I_{ON}/I_{OFF}
Si-C1C6C8-DPP-C5	6.50×10^{-3}	3.01×10^{-3}	−8.1 ± 2.0	$\sim 10^6$
5% c-SPB	0.57	0.20	−5.7 ± 2.4	$\sim 10^5$
10% c-SPB	0.75	0.48	−4.4 ± 1.6	$\sim 10^5$
50% c-SPB	0.88	0.62	−3.3 ± 1.8	$\sim 10^4$
Si-C1C6C8-DPP-C0[a]	2.89	1.35	−2.6 ± 1.0	$\sim 10^4$

[a] Drop-casted films.

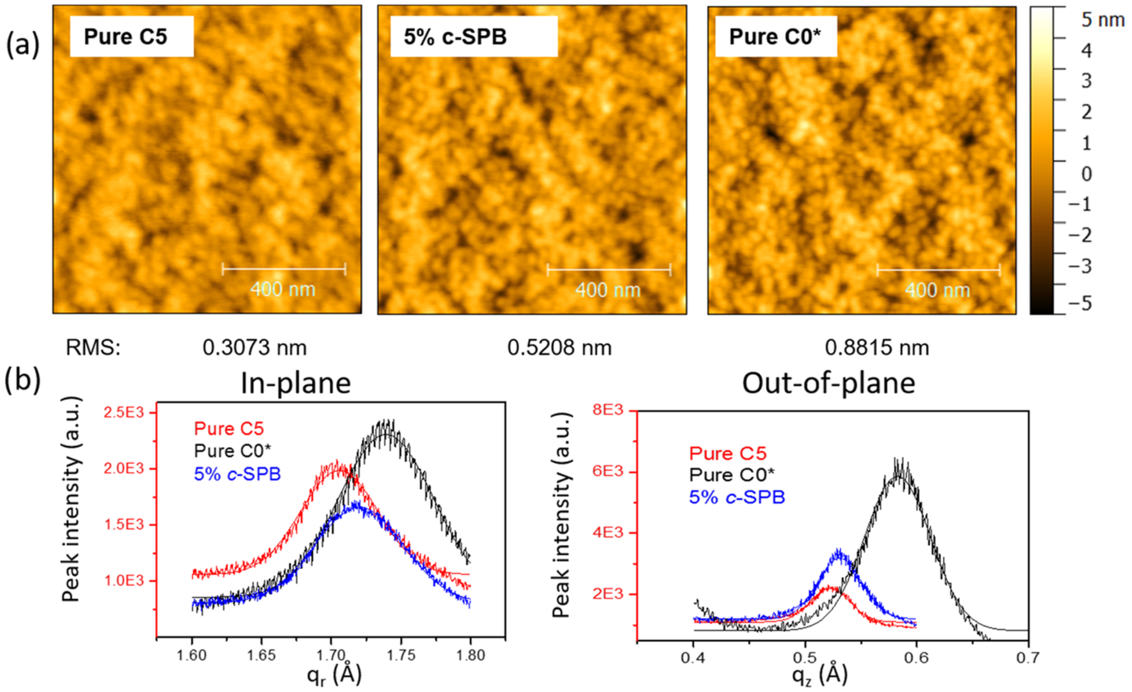

Figure 3. (a) AFM height images of the melt-processed thin films. (b) Selected peak line cuts of 2D diffraction patterns for comparison of in-plane π-stacking peaks and out-of-plane lamellar stacking peaks for pure Si-C1C6C8-DPP-C5, 5% c-SPB, and Si-C1C6C8-DPP-C0 (* indicates drop-casted film).

To yield a thin film, the dry polymer blend pellets were deposited on a cleaned and OTS-modified Si/SiO$_2$ and then sandwiched using a secondary clean substrate. The assembly was then allowed to fully melt at 130 °C while being pressed using a heavy object (10 kN/cm^2) for 2 h. Upon delamination, the thin film was transferred onto a cleaned and OTS-modified Si/SiO$_2$ substrate with Au electrodes to fabricate OFET device. To establish intimate contact between the substrate and the laminated films and eliminate any surfaces defects, the devices were placed on a hot plate (at 100 °C for an extra 15 min). For the devices based on the pure fully conjugated polymer, because the polymer could not be melted, the OFET devices were fabricated by drop casting, followed by a hot-pressing step at 130 °C for comparison. All OFET devices were then allowed to cool to ambient prior to electrical properties measurements. In the same manner, thin films used for atomic force microscopy (AFM) and grazing incidence X-ray diffraction (GIXRD) were prepared for further analysis.

The blending efficiency was studied using the 5, 10, and 50% c-SPB-based OFET devices. The representative OFET performance parameters are summarized in Table 2. Due the persistent dual-slope commonly observed for the DPP-based polymers,[12,28] the mobility values were evaluated in both low- and high-gate-voltage regimes; the calculated mobilities for higher-gate-voltage regimes are summarized in Table S1. The corresponding characteristic transfer and output curves are provided in Figure S6 along with dual sweep hysteresis analysis. Pure Si-C1C6C8-DPP-C5 showed a maximum mobility of 6.5×10^{-3} cm^2/(V s), whereas Si-C1C6C8-DPP-C0 could reach mobilities up to 2.89 cm^2/(V s) for a drop-casted film.

The charge-carrier mobility could be boosted by 2 orders of magnitude when as low as 5% of Si-C1C6C8-DPP-C0 was added. The mobility values then plateaued upon further increase of the amount of the added tie chains, as shown in Table 2. The c-SPB containing 50% of DPP-C0 showed hole mobility values reaching as high as 0.88 cm^2/(V s) when melt-pressed at 130 °C. Other parameters, including the threshold and the I_{ON}/I_{OFF} current ratios, were also moderate, as shown in Table 2. The addition of a small portion of the rigid tie-chain polymer in the blend showed to be sufficient to increase the electronic properties of the matrix polymer, as seen in other DPP-based blends.[28,35]

Morphology Studies. To elucidate the charge-transport efficiency in the melt-processed devices and investigate the miscibility of polymers upon melt crystallization, morphology studies as well as molecular packing analysis in thin films were conducted using AFM and GIXRD. The topographic images showed that the melted films were smooth upon delamination

(Figure 3a). No detectable phase separation between the two polymers could be observed, which is in a good agreement with the DSC data. These morphology behaviors were not surprising, as from Figure 2a, all of the thin films showed a metallic luster after melt pressing. This film smoothness was desired for the transfer and lamination step to ensure intimate contact between the film and the substrate. The free-standing films (Figure 2a) could thus be easily used in the lamination step as opposed to noncomplementary systems, where the dual-layer formation would require extra steps to access the semiconducting layer.[24] The in-plane and out-of-plane two-dimensional (2D) GIXRD diffraction patterns as well as the corresponding one-dimensional (1D) curves are shown in Figure S7. Key peaks extracted from the 1D curves comparing the crystallinity of the pure matrix, the 5% c-SPB, as well as the pure tie polymer are shown in Figure 3b. Even though spin casting is normally preferred for polymer diffraction studies, thicker (~1.5 μm) melt-processed films were chosen here to gain insights into the packing mechanism upon melting and cooling. For the same reason, drop-casted and hot-pressed Si-C1C6C8-DPP-C0-based films were used for a comparison. The melt-processed and thus thicker films based on Si-C1C6C8-DPP-C5 and 5% c-SPB gave ringlike diffraction patterns that indicated a broad distribution of out-of-plane orientation of crystalline aggregates. However, lower degree of out-of-plane alignment is not intrinsic to melt-processed films but is instead attributed to lack of confinement in thicker films. Therefore, much thinner spin-cast films were utilized for comparison and used to validate the extracted peak positions (Figure S7). From the 2D patterns of the melt-processed thin films, representative crystallography parameters were carefully extracted and summarized in Table 3.

Table 3. Crystallography Parameters for Melt-Processed Thin Films of Si-C1C6C8-DPP-C5, 5% c-SPB, and Si-C1C6C8-DPP-C0

material	$\pi-\pi$ spacing (Å)	in-plane FWHM (Å^{-1})	lamellar spacing (Å)	out-of-plane FWHM (Å^{-1})
Si-C1C6C8-DPP-C5	3.68	0.065	24.7	0.042
5% c-SPB	3.65	0.074	23.7	0.046
Si-C1C6C8-DPP-C0[a]	3.61	0.080	21.5	0.070

[a] Drop-casted thin film.

Si-C1C6C8-DPP-C5 showed an in-plane $\pi-\pi$ stacking peak appearing at 1.70 Å^{-1} corresponding to a packing distance of 3.68 Å. A $\pi-\pi$ stacking could also be observed in the out-of-plane direction at 1.70 Å^{-1} due to the large thickness of the film, as previously mentioned. Also along q_z, a (100) lamellar stacking peak could be found at 0.258 Å^{-1} corresponding to a *d*-spacing of 24.70 Å. This large lamellar spacing was expected because the spacer group along the polymer chain was intentionally made long, and bulky side chains were used.[32] Hot-pressed Si-C1C6C8-DPP-C0 showed a clear edge-on orientation with a well-defined $\pi-\pi$ stacking peak at 1.74 Å^{-1}, corresponding to a shorter *d*-spacing of 3.61 Å. The lamellar stacking peak appeared around 0.291 Å^{-1} corresponding to a *d*-spacing of 21.52 Å. Upon blending the two polymers in a 5% c-SPB, the GIXRD patterns showed a weak edge-on orientation with the in-plane $\pi-\pi$ stacking peak around 1.72 Å^{-1} corresponding to a packing distance of 3.65 Å. The out-of-plane lamellar peak moved to 0.266 Å^{-1} with a *d*-spacing of 23.69 Å. The presence of the small fraction of Si-C1C6C8-DPP-C0 in the blend thus shortened the $\pi-\pi$ stacking distance as well as the lamellar spacing by 0.04 and 1.01 Å, respectively. This close packing in c-SPB contributed to the increase in hole mobility by 2 orders magnitude in the 5% c-SPB in addition to the formation of tie chains. It could be concluded that not only does the tie-chain polymer serve as a connecting bridge between crystalline domains of the matrix polymer,[36] but also it also seems to play a crucial role in the melt crystallization of the blend. This behavior had previously been observed in a similar DPP-based system using in situ temperature-dependent GIXRD analysis[28] and could thus rationalize the increase in charge-carrier mobility.

■ CONCLUSIONS

We demonstrated the melt processing of complementary semiconducting polymer blends at 130 °C. The blend gave hole mobilities as high as 0.88 cm^2/(V s) with low threshold voltages and high I_{ON}/I_{OFF} ratios in hot-processed and laminated OFET devices. The low melting temperatures were achieved by utilizing asymmetrical solubilizing side chains in combination with an elongated conjugation break spacer. Morphology studies were used to elucidate the observed high charge-carrier mobility in the polymer blends. This processing of organic semiconductors at unprecedented low temperature renders this method adaptable to ubiquitous plastic substrates and significantly lowers the energy consumption. This design thus opens up opportunities in solvent-free processing as a more suitable route for low-cost and large-area formation of semiconducting thin film and organic electronic manufacturing.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.7b19847.

Detailed physical characterization experiments (PDF)

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Notes

The authors declare no competing financial interest.

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